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CONFORMAL/PLANAR ARRAY SONAR PROJECT (DEPENDABILITY ASSURANCE P--ETC(U)
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CONFORMAL/PLANAR ARRAY SONAR PROJECT

(Dependability Assurance Program)

Microelectronics Failure Rate Analysis

Lab. Project 920-72-6 Technical Memorandum #5

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Abstract

A realistic failure rate governing the use of micro circuit devices in the ESS installation and prototype system of the Conformal/Planar Array Sonar is developed. It is shown that a serious discrepancy exists between failure rate data generated by producers and user agencies. Procedures for R and M assurance are recommended.

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1.0 Administrative Information

By reference (a) the Naval Applied Science Laboratory (NASL) was assigned responsibility for the development and implementation of a dependability assurance program for the Conformal/Planar Array Sonar Project. As part of this program, NASL was authorized by reference (b) to recommend an electronic hardware approach for use with the Expermental Sonar Ship (ESS) installation. The planned effort described herein is covered by PERT Event 0863 of the current NASL PERT chart shown in reference (c) and Task 1240 of reference (d).

This memorandum is concerned with the development of a realistic failure rate for the microelectronic components that will be utilized in the subsystems and equipments comprising the Conformal/Planar Array Sonar which is presently in the Concept Formulation phase of the system development cycle. The intent is to provide failure rate values which may be utilized with confidence in connection with the reliability and availability modeling tasks being performed at the Naval Applied Science Laboratory. The first application will be to provide an input to the reliability model of the "transmit," function as agreed at November 1-4, 1966 technical meetings held at San Diego, California. The concept of this portion of the system has hardened to the point where the microelectronic components have been selected or are in process of development. As the design concepts evolve, this data will also be applied to other functions involving the use of microelectronics.

Acknowledgment is made to the System Design Techniques and Analytic Techniques Groups of the SPE Branch and to the Maintainability Engineering Branch for assistance in the preparation of this memorandum.

1.1 References

(a) BUSHIPS ltr 9674 Ser 1623-21 of 14 Jan 1965
(b) NEL ltr Ser 2110-318 of 10 Dec 1965
(c) August-September Status Report NASL ltr 921-EVO:rr Lab. Project 920-72-6 Monthly Report of 27 Oct 1966
(d) "Plan for NASL Participation in the C/P Array Sonar Systems Effectiveness Effort During Concept Formulation" 1 Oct 1966
(e) Draft DOD Memorandum, "Proposed Policies for Use of Microelectronics in Military Systems and Equipment," of 31 Mar 1966 with comments by Adm. F. L. Pinney, Jr. memo to DDRE of 6 May 1966
(f) "The Feasibility of Micropower Microelectronics for Shipboard Functions," Final Report of 4 Oct 1965; prepared for U.S. Naval Applied Science Laboratory Contract N140 - (62462) 7739-8B
(g) MIL-HDBK-217A Reliability Stress and Failure Rate Data for Electronic Equipment
(h) RADC Specification 2867 of 5 Oct 1966 "Quality and Reliability Assurance Procedures for Monolithic Microcircuits"

(i) Memo on Integrated Circuit Failure Rates prepared by TRG (Undated)
(j) NASL ltr 921-EVO:rr Lab. Project 920-72-6 Monthly Status Report of 23 Feb 1967
(k) MIL-STD-736A(Ships) Military Standard Unitized Equipment Design
(l) "Handbook for Systems Application of Redundancy" of 30 Aug 1966, NASL Publication

1.2 Background Information

Special consideration, as required by reference (e) is being given to the utilization of microelectronic devices in advanced systems under development throughout the Department of Defense. Although, a large body of data relative to failure rate and failure rate characteristics of microelectronic devices has been compiled in the relatively short time these devices have been in use, the published data exhibited such a wide variation in range as to be of little value in its present form. This memorandum therefore is concerned with the analysis of the available data with a view to the development of a realistic mean failure rate that can be utilized with confidence for reliability and maintainability prediction purposes by technical and management personnel.

The transmit beam former proposed for the C/P Array Sonar consists essentially of a switching matrix whose function is to transfer amplitude and phase information to each of the approximately 2700 transmit modules used to energize each array. Since there may be as many as several hundred transmit beams generated (each requiring a different combination of amplitude and phasing data) the information required for each beam will necessarily be stored in some form of memory. For the proposed design the basic circuit will be a type D flip-flop. This circuit will be employed to provide the storage register, shift register and binary counter functions that will be required. In order to provide continuous availability in case of a part breakdown, a combination of triple redundancy and majority logic will be utilized. It is estimated that a total of approximately 16000 microelectronic chips will be required for the transmit beam former function.

For purposes of the Experimental Sonar Ship (ESS) two types of microcircuit modules designated as the preset counter module and the shift register will be required as the basic building blocks for the transmit beam forming function. The flip-flop modules required for the register functions are obtainable commercially from off-the-shelf sources. Because of its configuration, and in order to reduce bulk, the preset counter module will require engineering development. A contract for this purpose has been awarded by GD/E to the Molecular Electronic Division of Westinghouse.

2.0 Object

The primary objective of this analysis is to derive a realistic failure rate for the microelectronic components and devices proposed for use in the Conformal/Planar Array Sonar. A secondary objective is to establish the constraints with respect to the applicability of the derived failure rate and to recommend reliability and maintainability assurance procedures governing the use of microelectronic devices in this project.

3.0 Procedure

The procedure utilized in arriving at a realistic microelectronic failure rate was based on the temperature dependence characteristics of semi-conductor devices. The derived rate was determined by taking into account the environmental conditions under which the Conformal/Planar Array Sonar would be required to operate. The basic data for the determination of this failure rate was obtained from references (f) and (g).

4.0 Theoretical Considerations

The pertinent consideration involved in the failure of microelectronic and solid state devices is as follows:

a. Failure rate is a function of junction temperature. This assumes that the manufacturing process has been debugged to the point where failures due to faulty manufacturing techniques have been minimized to the greatest extent possible.

b. Junction temperature is determined by the combined effects of the ambient temperature in which the device is operated, the rate of heat generation at the junction and the rate at which the generated heat is dissipated.

c. Heat generation is a function of the power consumed at the junction.

d. Heat dissipation is a function of the method of cooling. The heat may be dissipated by convection, conduction or radiation. "Natural" cooling generally combines all three techniques while "forced" cooling requires the circulation of air (gas) or liquid (water) around the device being cooled.

5.0 Results of Microelectronic Feasibility Studies

In the microcircuit feasibility studies, reference (f), the actual relationship between the failure rate of microcircuit devices and operating temperature was established within 60 percent confidence limits from data provided by three manufacturers of microcircuit components. The results obtained are shown in Figure 1. It will be seen that the characteristics based on Mfrs "B" and "C" data were in relatively close agreement while that based on Mfr "A" data was considerably more pessimistic exhibiting a relatively narrow change in failure rate as a function of temperature. This lack of agreement on the part of the Mfr "A" data would indicate that temperature may not have been the controlling failure mechanism. Hence the Mfr "A" data was considered inconclusive and therefore was rejected for purposes of this analysis. Of the remaining characteristics, the one provided by Mfr "C" (the more optimistic of the two) was selected as the applicable characteristic for the purpose of this analysis on the basis that failure rate should decrease as manufacturing techniques are refined. For purpose of this analysis, the Mfr "C" characteristic is shown in Figure 2 and will provide the basis for selection of the characteristic microelectronic device failure rate for the Conformal/Planar Array Sonar derived below.

5.1 Conformal/Planar Array Operating Ambients

The general specification governing the design of the Conformal/Planar Array Sonar is MIL-E-16400. With the exception of the array proper and the connecting cables all equipment will be installed below deck. Hence the class 4 temperature of 0 to 50 degrees Centigrade as defined in MIL-E-16400 will apply. However, the controlling temperature with respect to failure rate is the junction temperature existing within the microcircuit device. To the equipment ambient temperature (T_e), therefore, must be added the temperature differentials between the equipment ambient and the module ambient (T_m) and the differential between the module ambient and the junction (T_j). In other words:

$$T_j = T_e + \Delta Tm + \Delta T_j$$

where $\Delta T_m = T_m - Te$

$$\Delta T_j = T_j - T_m$$

For purposes of this analysis ΔTm was assumed to be 20 degrees Centigrade and ΔT_j was assumed to be 33 degrees Centigrade as recommended in reference (f). The latter value was based on a maximum permissible heat flux of 0.25 watt per square inch of surface area for natural cooling. Forced air or other means of forced cooling will be required for higher rates of heat generation.

5.2 Failure Rate Determination

Taking the above temperature and temperature differentials into account and relating the derived junction temperature to the characteristic shown in Figure 2, the appropriate failure rate may then be chosen. For prediction purposes, the failure rate was determined from the following:

Highest (worst case) junction temperature = 50 + 20 + 33 = 103°C
Lowest (best case) junction temperature = 0 + 20 + 33 = 53°C
Mean = 78°C

Failure Rate corresponding to mean junction temperature (refer to Figure 2) $= 0.31 \times 10^{-6}$

The justification for using the "mean" rather than "worst case" is based on the following considerations:

a. Although ambient temperatures may vary considerably at any given time over a year's time, the long term average of 25°C will usually apply.

b. It is not likely that the maximum ambient of 50°C will apply for an extended period of time.

5.3 Analysis of MIL-HDBK-217A Data

A failure rate of 0.4 failures per million hours was recommended as a best estimate in MIL-HDBK-217A. The result obtained by the analysis based on reference (f) therefore was in close agreement with the most recent findings of MIL-HDBK-217A. Similar data presented in an earlier edition of MIL-HDBK-217A is presented in Figure 3. Reference to this figure shows that for a ratio of operating to nominal rated power of 0.38 (62 percent derating), the failure rate for a junction temperature of 78°C will be 3.1 failures per million hours which is ten times that shown by Figure 2. However, this result was based on "as received" lots of components. By resorting to a single measurement screening involving temperature cycling, centrifuge and steady state operating life tests, the failure rate will be reduced to one-tenth that of the unscreened lot. The "screened" failure rate therefore becomes 0.31 failures per million hours which is in agreement with the result derived from Figure 2. Thus in order to achieve a high degree of reliability it will be necessary to resort to suitable screening tests in order to weed out unreliable components prior to assembly on the modules. It may therefore be concluded that a failure rate of 0.3 failures per million hours represents a realistic failure rate based on present state-of-the-art manufacturing capabilities.

5.4 Comparison of Producer/User Failure Rate Data

Table 1 illustrates the discrepancy that exists between the failure rates obtained by producers with failure rates obtained under actual operating conditions by independent testing agencies. Failure rates obtained by the producer are shown to vary between 0.019 and 0.14 failures per million hours while failure rates as determined under operating conditions are shown to range between 0.21 and 1.80 failures per million hours depending on operating temperatures or temperature cycling. These results confirm that the failure rate value of 0.3 failures per million hours is a realistic one and also show that screening is required to achieve this value.

5.5 Other Studies

An independent analysis of the problem, summarized in reference (i), came to essentially the same conclusion as this analysis with respect to present state-of-the-art manufacturing capabilities. In reference (i) it was also indicated that by extrapolating present capabilities into the 1970 era, an anticipated reasonable failure rate at that time would be 0.01 failures per million hours. Available data however suggests that this value approaches perfection and hence represents an irreducible minimum. Therefore, if it is assumed that the order of magnitude discrepancy between producer and user data will remain unchanged then a more realistic rate would be 0.1 failures per million hours. In order to assure achievement of this performance, a high degree of screening would still be required.

5.6 Connection Reliability

In addition to the reliability of the microcircuit device, another factor of concern is the reliability of the connections between the microcircuit device or "chip" and the card or module to which the device is connected. There are various techniques available for making these connections. MIL-HDBK-217A lists the relative reliabilities of the various techniques in order of increasing failure rate as follows:

a. wire wrap
b. weld
c. machine solder
d. crimp
e. slip fit
f. hand solder

However the only data given in reference (g) for operating conditions that most nearly approximate shipboard environment is with respect to machine solder connections. The value given was 0.034 failures per million hours per connection.

6.0 Discussion

On the basis of the extremely high reliability claimed for microelectronic devices, it would appear that the failure rates of 0.3×10^{-6} and 0.1×10^{-6} that have been designated for the ESS installation and prototype system are somewhat conservative. The decision to use these values are, however, considered justified in view of the order of magnitude discrepancy between producer claims and user experience as has been noted. Recent criticism leveled at the industry also emphasize this discrepancy. In general, it should be noted that the reliability obtained with these devices was the result of careful quality control on the part of the producer and of intensive screening by both producer and user. The point to be emphasized is that high reliability can be achieved by screening tests designed to weed out potentially unreliable units.

Recent reliability studies completed on the transmit function subsystem, reported in reference (j), indicated that on the basis of the 0.3×10^{-6} and 0.034×18^{6} failure rates assigned to the microelectronic devices and associated wire connections respectively, the expected mean life for the redundant portions would be 967 hours. Exercising of the reliability model indicated that any further reduction in the microcircuit failure rate would not significantly increase the mean life value that was obtained for the above system. The conclusions therefore are:

a. Microcircuit devices have achieved a high degree of reliability at least for the transmit function.

b. Reliability improvement efforts should be concentrated on other areas associated with the beamformer such as the serial elements of the subsystem.

c. Microcircuit reliability must be maintained at the specified level by resorting to quality control and screening techniques.

The magnitude of the logistics and maintenance problems relative to the transmit beamformer may be estimated from the following analysis. It may be arbitrarily assumed that the sonar system, of which the transmit beamformer is a part, will be operational 6000 hours in any given year. This represents a 70 percent utilization factor. On the basis of a constant failure rate of 0.3×10^{-6}, the number of failures per year will be:

$$F = n \lambda t$$

where F = no. of failures
n = no. of microcircuit chips
λ = failure rate, failures per hour
t = time, hours

$$F = 16000 \times 0.3 \times 10^{-6} \times 6000$$
$$= 28.8 \text{ failures per year}$$
$$\text{or } 2.4 \text{ failures per month}$$

If connection failure is considered, the failure rate would be dependent on the number of input/output and control connections. As a minimum the failure rate of the chip including the connections would be at least twice that of the chip alone. Hence a failure rate of the order of a minimum of 5 failures per month for the transmit beamformer may be expected.

6.1 Alternate Approaches

Two alternate approaches to the overall problems of reliability and maintainability from the standpoint of cost and logistics are available:

a. Multifunction Circuit (MFC) Approach. This approach involves the use of modules having multifunction capabilities. The advantages would be reduced cost and spares requirements. This technique is within present state-of-the-art capabilities. A multifunction circuit may be defined as a group of partially connected active and passive components that may be caused to operate in any one of several functional modes by means of external programming. The internal realization of the functional modes is achieved by the completion of one of several alternate interconnection patterns. For even greater versatility, externally located adaptation circuits will provide an adaptable multifunction circuit capability.

b. Self-Repair Capability. This approach would involve configuring the system in such a way as to provide automatic fault detection and location with faulted module replacement. Although self-repairable systems are not wholly within the state-of-the-art, such a development would provide the means for enhancing reliability, improving maintainability and simplifying support requirements by reducing the need for spare parts provisioning. The considerations leading to the desirability of a self-repair capability are given in Appendix A.

7.0 Reliability and Quality Assurance Procedures

To assist in establishing the required screening of the microcircuit devices required for the Experimental Sonar Ship (ESS), the procedures outlined in reference (h) are tentatively recommended. These procedures were developed for the Air Force Systems Command for the procurement of monolithic microcircuits. With little or no modification they may be utilized to establish quality and reliability assurance procedures that are applicable to the ESS and to the prototype system. A copy of reference (h) is attached hereto as Appendix B.

7.1 Maintainability Assurance

From the system design standpoint, the microcircuit devices will be wired into modular assemblies or modules, the lowest replaceable unit. Therefore with respect to maintainability assurance, it is recommended that the system design be guided by the design objectives given in reference (h) for the design of unitized equipment. Since maintenance will be by module replacement to the greatest extent possible, it will be necessary to make provision for off-line testing and repair facilities. The decision whether or not to repair modules will be determined largely by economic factors. Development of a support system capable of operating in a hostile environment will make the throwaway concept feasible. If not, development of a repair capability will be required. For this situation, there will be specific needs for:

a. Development of module or assembly test devices or equipment capable of locating the failed microcircuit device.

b. Development of personnel skills and wiring techniques for the removal and replacement of the failed device from the module.

8.0 Recommendation

Availability Model. The recommended microelectronic device failure rates for use in the reliability and availability models being developed for the Conformal/Planar Array are as follows:

System	Applicable Time Frame	Microelectronic Chips	Microelectronic Connections
ESS Installation	1968 - 1970	0.3×10^{-6}	0.034×10^{-6}
Prototype	1970 - 1980	0.1×10^{-6}	0.034×10^{-6}

It should be noted that the failure rate for the microelectronic connections will be reduced drastically as interconnection techniques are improved. The value covering the microelectronic connections should be updated as the information becomes available.

R and M Assurance. The recommended documentation with respect to reliability and maintainability assurance are:

a. RADC Specification 2867 of 5 October 1966, "Quality and Reliability Assurance Procedures for Monolithic Microcircuits"

b. MIL-STD-736(A)(Ships), Military Standard "Unitized Equipment Design"

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Figure 1 - Failure Rate Characteristics of Microelectronic Devices Based on Data Provided by Three Manufacturers

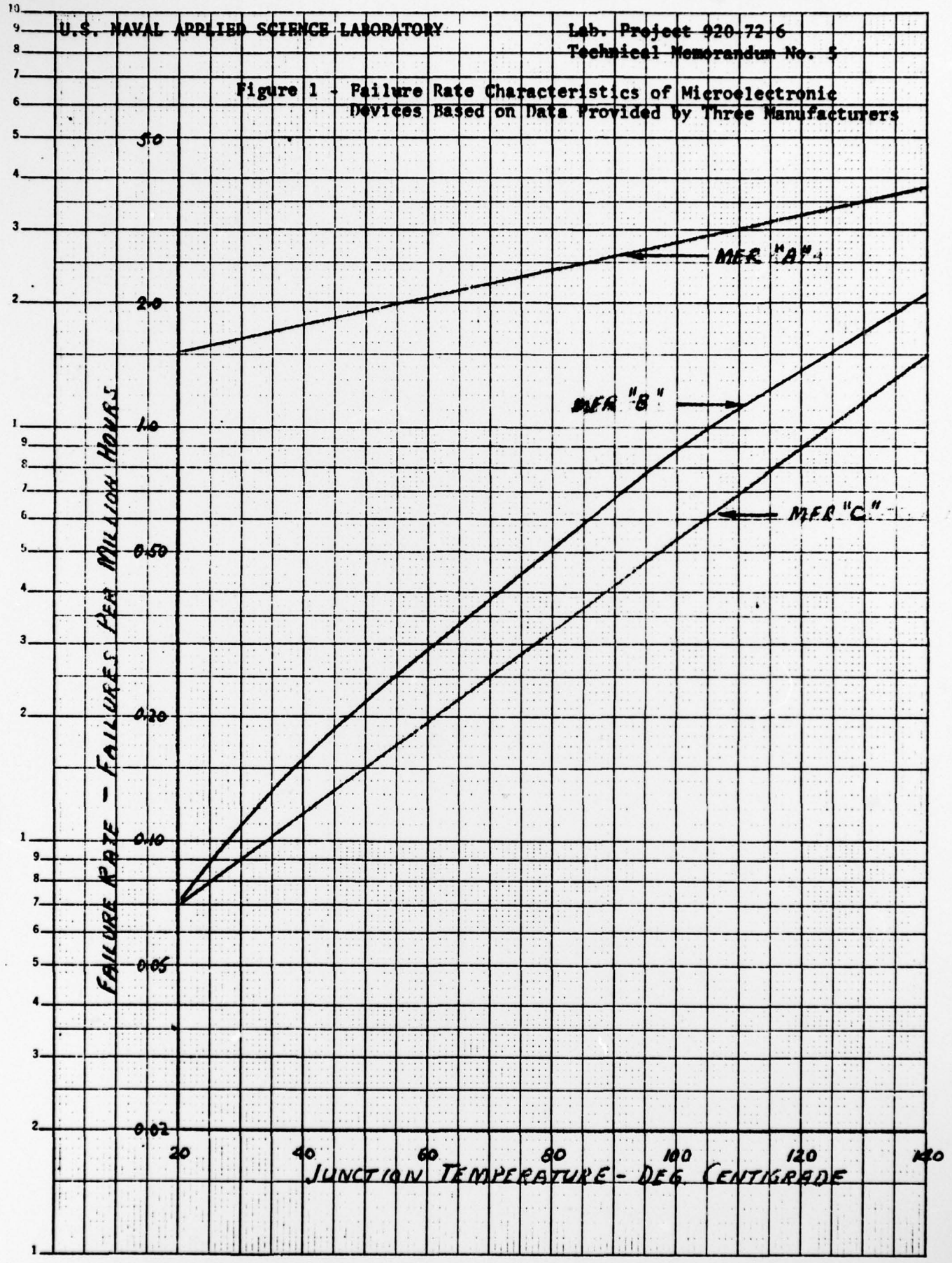


Figure 2 - Determination of Microelectronics Failure Rate Applicable to Shipboard Environment

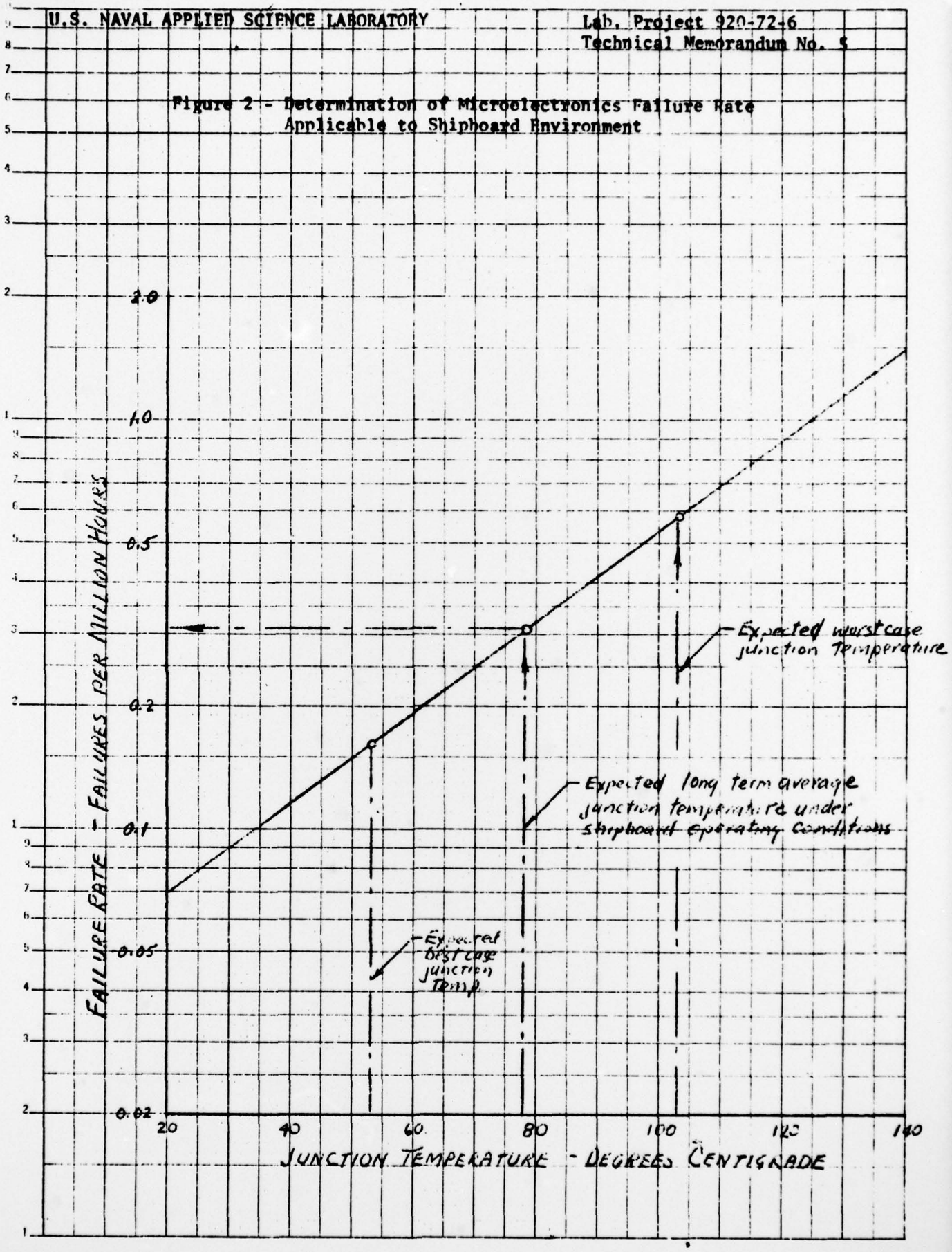
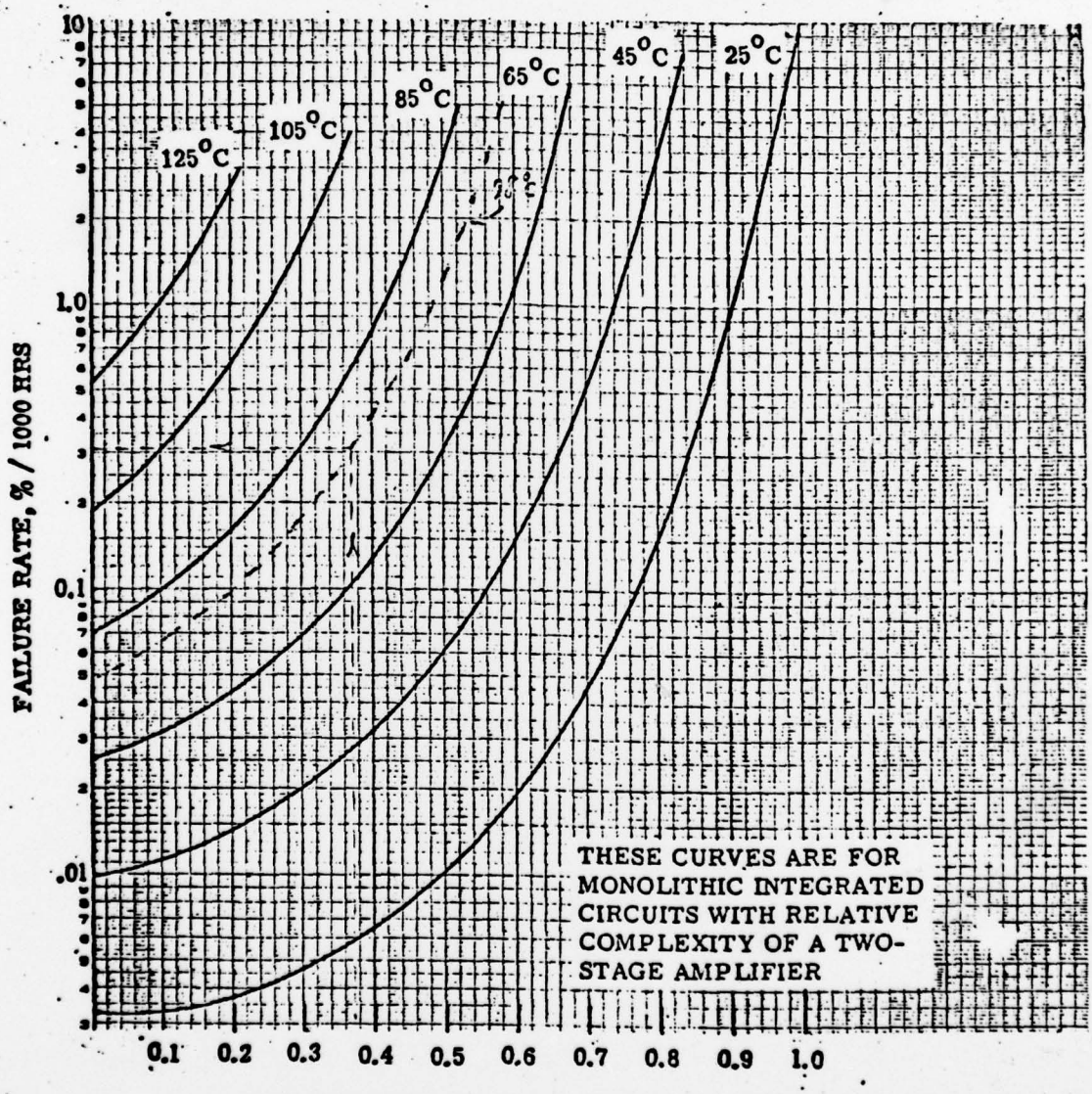


Figure 3 - Failure Rate of Monolithic Integrated Circuits
As a Function of Power Dissipation and Temperature

MULTIPLY FAILURE RATE BY ALL APPLICABLE FACTORS BELOW:

MULTIPLE-CHIP INTEGRATED CIRCUITS	5.0
SINGLE MEASUREMENT SCREENING (TEMP. CYCLING, CENTRIFUGE AND STEADY-STATE OPER. LIFE)	0.1
SINGLE MEASUREMENT SCREENING (TEMP. CYCLING, CENTRIFUGE AND HI-TEMP LIFE (NON-OPER.))	0.2

NOTE: USE NO FINAL FAILURE RATE BELOW 0.001 %/1000 HRS.



* DEFINED AS THE RATIO OF DISSIPATED POWER TO NOMINAL RATED POWER FOR THE ENTIRE INTEGRATED CIRCUIT PACKAGE OR THE RATIO OF DISSIPATED POWER TO NOMINAL RATED POWER FOR ANY SINGLE TRANSISTOR IN THE CIRCUIT, WHICHEVER IS GREATER. FOR A SINGLE TRANSISTOR, USE NOMINAL POWER RATING WHICH THE EQUIVALENT SINGLE TRANSISTOR TYPE WOULD HAVE IF PACKAGED AND MOUNTED IN THE SAME MANNER AS THE INTEGRATED CIRCUIT.

TABLE 1

SUMMARY OF TYPICAL INTEGRATED CIRCUIT FAILURE RATE STUDIES
REPORTED BY PRODUCER AND USER AGENCIES

Source	Manufacturer	Test Time (Device-Hours)	Temperature Deg. Cent.	Failure Rate at 60% Confidence $F/10^6$ Hours	Remarks
CBS Labs Report (Reference (f))	C	1.37×10^6	25	0.07	Failure Rate Normalized to 25°C
	A	7.17×10^6	25	0.05	Failure Rate Normalized to 25°C
	B	9.4×10^6	25	0.10	Failure Rate Normalized to 25°C
	D	50×10^6	--	0.019	Apollo Microcircuits
	D	30×10^6	125	0.14	Non Epitaxial Micro logic
	D	25×10^6	125	0.04	Epitaxial Micro logic
MIL-HDBK-217A (p.7.15-4)	-	19×10^6	*	0.50	Results of special tests on digital modules performed by independent tes agency
(p.7.15-4)	-	577×10^6	25	0.21 (Note 1)	Microrac system tested under normal operating conditions
(p.7.15-5)	-	24.5×10^6	85**	1.71 (Note 2)	Digital micro module life test under normal operating conditions
(p.7.15-5)	-	16.8×10^6	125**	1.80 (Note 3)	Digital micromodule life test under normal operating conditions

* Temperature cycled, 50 hours at -54°C, 400 hours at 80°C
** Junction Temperature

NOTES: (1) Failure rate obtained from Figure 2 for this temperature would be 0.08 $F/10^6$ hours
(2) " " " " " " " " " " " " 0.37 $F/10^6$ "
(3) " " " " " " " " " " " " 1.00 $F/10^6$ "

Appendix A - Considerations Relative to the Development of Self-Repairable Systems

1. Introduction. Studies are currently underway the objectives of which are to provide the Conformal/Planar Array with a self-test and fault location capability. This area is considered to have a high probability of success since the techniques for providing this capability are known and are within the state-of-the-art. The Navy has already had notable success in this area with respect to the E-2A airborne tactical control system. In addition, the specifications for the current F-111 program now require self-test while in flight. Thus the self-test concept is finding increasing acceptance. In essence, the self-test concept calls for continuous on-line performance monitoring so that when a failure occurs within the system it will be identified quickly and corrected while the system is in operation. However the self-test routine can only point to the particular module or assembly where the failure has occurred. The actual replacement must still be accomplished by a technician who will remove the faulted module and replace it with a satisfactory module. This concept is therefore dependent upon the availability of maintenance personnel and replacement parts. The next step logically would be to design the system in such a way that the repair or replacement would be effected automatically, in other words, a self-repairable system.

2. Basic Considerations. The design of every system has attributes governing its performance with respect to time. These attributes are generally expressed by such measures as reliability, availability, maintainability and dependability. The initial concern of the system designer, however, is to provide performance to fulfill an assigned function or mission. As the system takes shape the next item of concern is the maintenance of the required level of performance with respect to time, i.e. reliability, maintainability, and so on. Thus the possibility of aging of component parts or of catastrophic failure must be evaluated and any undesirable characteristics minimized or eliminated where possible. Thus collaboration with the reliability engineer will generally result in modifying the system design in order to provide the desired performance with respect to time.

3. Reliability Engineering Considerations. The approach taken by the reliability engineer in evaluating particular system designs is based essentially on a combination of analysis and experience. Analytic techniques are required to develop both the reliability requirements and to develop system availability models. When the experience factors are taken into account, the combination then forms the basis for reliability prediction and verification. However, the accuracy of this technique is dependent upon the validity of the input data. Thus the availability of accurate failure data and a basic understanding of the mechanism of failure are essential ingrediants of reliability implementation.

4. Impact of Microelectronics. Since the advent of semi-conductors and more recently of monolithic integrated circuit and microelectronic devices there has been an explosive increase in the potential for improvement with respect to reliability and the other time dependent measures. However commensurate with the increased reliability there has been a corresponding increase in complexity so that on an overall basis system reliability has increased but at a slower rate. To date, the emphasis has been toward higher reliability and more rigid reliability assurance techniques. Because of this trend, reliability validation is becoming increasingly costly and time consuming. As an example, to demonstrate a failure rate of 0.1 failure per million device-hours with 90 percent confidence (which is attainable with the present state-of-the-art) it would be necessary to test 93000 units for 1000 hours or 9300 units for 10000 hours with not more than 5 failures in either case. That this high degree of reliability is attainable indicates that the mechanism of failure is well understood and that the process and quality control procedures are highly developed. As a matter of fact the technology has advanced with such rapidity that developments in progress will result in automatic computer aided control of the entire process beginning with the initial concept through to the production phase of the desired monolithic structure. Thus the development of a self-repairable system is within present capabilities of the art. For detailed information with respect to the self-repairable system concept the reader is referred to reference (1) (Section 6, Handbook for Systems Application of Redundancy).

5. Conclusion. The self-repairable system concept should make it possible for the design to absorb the cost of the built-in spares. In addition this concept should make it possible to record time of failure, thus providing an exact record of the incidence of failure and also of maintenance actions. It would therefore be possible to pinpoint trouble areas from the statistics recorded in the data bank in which the failure data was recorded. In effect, we are presented with the capability of an integrated approach to the problems of reliability, maintainability and logistics. In conclusion, the advantages to be derived from a self-repair capability are as follows:

a. Repairability. The manual repair function will be replaced.

b. Sparing. Spares are incorporated in the original system procurement.

c. Reliability Enhancement. A relatively small number of components will provide added reliability since each back-up component can be assigned to several components rather than providing back-up on a one-for-one basis.

d. Versatility. The back-up components may be used to perform an active or monitoring function until needed for replacement.

e. Self-check. Operating and back-up components may be tested periodically to ascertain degradation with time.

f. Failure Recording. Time and location of failure may be recorded thus establishing failure incidence for verification of predicted reliability and to locate high rate failure areas.

APPENDIX B - PROPOSED SPECIFICATION FOR SCREENING MONOLITHIC MICROCIRCUITS

AIR FORCE SYSTEMS COMMAND
ROME AIR DEVELOPMENT CENTER

RADC Specification 2867
5 October 1966

QUALITY AND RELIABILITY ASSURANCE PROCEDURES FOR MONOLITHIC MICROCIRCUITS

1. SCOPE

1.1 This specification establishes the quality and reliability assurance procedures for monolithic microcircuits.

2. APPLICABLE DOCUMENTS

2.1 The following documents of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

STANDARDS

Military

MIL-STD-202	Test Methods For Electronic And Electrical Component Parts
MIL-STD-750	Test Methods For Semiconductor Devices

(Copies of documents required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Monolithic microcircuits shall be subjected to the quality assurance provisions specified in 4. herein. This does not preclude the performance of additional tests or inspections as may be required. It is not intended to prohibit normal production tests performed by the manufacturer of the microcircuits, but rather to supplement the tests.

4. QUALITY ASSURANCE PROVISIONS

4.1 Pre-cap visual inspection.- 100 percent in accordance with the requirements of "Visual Inspection Procedures and Criteria for Monolithic Microcircuits." as specified in Appendix A herein.

4.2 Stabilization bake.- 100 percent preconditioning of all devices at a temperature between 125 and 175°C for no less than 48 hours.

RADC Specification 2867

4.3 Temperature cycling.- 100 percent of all devices shall be subjected to 5 cycles of thermal shock in accordance with MIL-STD-202, Method 107 Test Condition B, or in accordance with MIL-STD-750, Method 1056.1 Test Condition A.

4.4 Centrifuge.- 100 percent of all devices shall be subjected to acceleration stresses of 30,000 G in the Y_1 direction in accordance with MIL-STD-750, Method 2006 or in accordance with MIL-STD-202, Method 212 Test Condition B.

4.5 Visual inspection.- 100 percent of all devices shall be subjected to external visual inspection at 30X magnification in accordance with MIL-STD-750, Method 2071.

4.6 Hermeticity

4.6.1 Fine leak.- 100 percent of all devices shall be subjected to leak test in accordance with MIL-STD-202, Method 112 Procedure IIIa, Condition C.

4.6.2 Gross leak.- 100 percent of all devices shall be subjected to leak test in accordance with MIL-STD-202, Method 112 Condition A, ethylene glycol. This test shall be conducted subsequent to the Fine Leak procedure of 4.6.1 and shall be conducted as indicated in Condition A, disregarding the substitution paragraph of MIL-STD-202, Method 112.

4.7 Zapp test.- 100 percent of all devices shall be subjected to the following electrical stress in order to force to failure "Pinhole Shorts" that exist between interconnect and substrate on devices prior to final electrical test.

4.7.1 Method.- All terminals that will assume a back bias except the ground terminal must have +40 volts DC from a constant voltage source applied through individual 1 megohm resistors. The ground terminal shall be referenced to electrical ground.

4.7.2 Alternate method.- All terminals that will assume a back bias shall be connected to electrical ground through individual 1 megohm resistors. The ground terminal shall have -40 volts DC applied from a constant voltage source.

4.7.3 Reject criteria.- Any device subjected to the stresses described in either 4.7.1 or 4.7.2 herein shall be rejected if there is any evidence of dielectric breakdown in the oxide. (NOTE: More than one test may be required to connect each terminal to achieve the back bias condition.)

4.8 Electrical test.- "Electrical Acceptance Tests," both in content and tolerances, are subject to wide variations in specification because of the variety of circuit types, equipment design and expected conditions of use. Furthermore, it is considered essential to the realization of maximum quality and reliability in the final equipment that the vendor and the user share responsibility for the guarantee of quality and reliability in the specific application by jointly concurring in the use conditions.

4.8.1 Device specification.- The prime contractor shall secure from the vendor a complete part specification for each microcircuit used in the equipment, detailing all parameters significant to the application including those employed in the quality and reliability assurance procedures for the program. This specification shall include all static and dynamic characteristics for all conditions of test and application in the program, and the rated limiting parameters and values which, if exceeded, would result in part failure. This specification shall become effective following specific approval by the procuring activity.

4.8.2 Electrical acceptance tests.- The part specification prepared in accordance with 4.8.1 herein shall be used as the basis for all Electrical Acceptance Tests conducted for the program. Any deviation in any parameter beyond the specified values and tolerances shall result in rejection of the part. Once rejected, no part may be retested for acceptance. All electrical acceptance tests shall be conducted twice. Only those parts which pass the first Electrical Acceptance Test shall continue into the second test sequence.

4.8.3 Electrical test sequence.- The required Electrical Acceptance Tests shall be conducted following the sequence of tests described in 4.1 through 4.8 herein and shall be conducted again following the burn-in procedure of 4.9 herein. At the discretion of the vendor, all or any portion of the Electrical Acceptance Tests may be conducted at any additional points in the test sequence for the purposes of parameter screening or other purposes.

4.8.4 Electrical test data reporting.- When required by the contract, for each lot tested, a report shall be submitted to the procuring activity indicating quantity of parts tested, lot number or date code, quantity of parts rejected, the specific cause(s) for rejection, and the quantity rejected for each cause.

4.9 Burn-in .- 100 percent of all parts shall be subjected to a burn-in screen of no less than 250 hours at a temperature of no less than 125°C. Transistor-Transistor Logic (TTL) circuit types shall be operated in a ring-counter configuration with all inputs exercised. For other logic types a power burn-in with appropriate reverse-bias conditions imposed on all input diodes shall be employed. The intent is to exercise at maximum rated conditions all elements of the microcircuits. Detailed operating conditions and procedures, including monitoring procedures shall be subject to the approval of the procuring activity. It is desirable that continuous or periodic monitoring of microcircuit performance be accomplished during burn-in and that data on time-to-failure of each part or failures per period be reported as a basis for observing screen-out rates or rate changes.

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4.9.1 Burn-in data reporting.- For each lot tested, a report shall be prepared indicating quantity of parts tested, lot number or date code, quantity of parts rejected, the specific cause(s) for rejection, and the quantity rejected for each cause. For continuous or periodic monitoring during burn-in data on time-to-failure or period during which failure occurred will be reported for each reject in addition to the data on cause and quantity.

4.10 Overall test sequence.- With the exception of variations specifically authorized herein, the test sequence shall be in the order presented. Any other variation in sequence or test procedures shall require the specific approval of the procuring activity.

4.11 Limit testing.- Sample quantities of each microcircuit type shall be drawn from each production lot for this program and subjected to destructive tests to establish the absolute limit of the stresses which the microcircuits can withstand and to identify the modes of failure involved. These tests shall include physical (mechanical and environmental) stresses, electrical (power, current, voltage, et cetera) stresses and combinations thereof appropriate to the intended use condition. Stresses shall be applied in appropriate steps up to the point where at least 50 percent of all samples fail the specific procedure. The specific procedures and sample quantities shall be subject to approval by the procuring activity.

4.12 Limit testing data reporting.- The distribution of failures by failure mode, stress level, time-to-failure for each part type and lot shall be reported to the procuring activity.

5. PREPARATION FOR DELIVERY.- Non applicable

6. NOTES.- Non applicable.

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APPENDIX A

VISUAL INSPECTION PROCEDURES AND CRITERIA FOR MONOLITHIC MICROCIRCUITS

10.0 SCOPE

10.1 This appendix establishes the visual inspection procedures and criteria for monolithic microcircuits.

20.0 REFERENCES - Non applicable.

30.0 REQUIREMENTS

30.1 Monolithic microcircuits shall be subjected to the visual inspection procedures and criteria as specified in 40.0.

40.0 QUALITY ASSURANCE PROVISIONS

40.1 Scratches (90X minimum magnification) - No scratches shall be acceptable which go completely through the metallization reducing its width by one-half or more. Scratches occurring in metallization contact cut areas shall not be acceptable if they leave one-half or more of the contact area isolated from the metallization strip. Scratches occurring on metallization bonding pads shall not be acceptable if they occur in such a manner as to isolate one-half or more of the ball bond from the metallization strip. Silicon oxide must be visible throughout the length of each scratch.

40.2 Bridge metallization (80X min.) - Reject all material on which the distance between two metallization strips has been reduced by 3/4 ths. or more the normal separation at that point or to less than a 1/4 of a mil. Such reduction may be caused by smears, photolithographic defects or conductive foreign material.

40.3 Corrosion (150X min.) No devices shall be acceptable with any evidence of metallization corrosion.

40.4 Voids (80X min.) - No device shall be acceptable exhibiting a void at an oxide step which reduces the width to less than 0.75 mils. No device shall be acceptable which contains a void reducing the width of the metallization at that point to less than 0.6 mils. No device shall be acceptable which reduces a pad by 50 per cent of its designed area or which appears to isolate more than 50 per cent of the ball bond from its associated metallization strip.

40.5 Foreign material (30X min.) - Unattached metallic, abrasive or conductive material on the surface of the die or within the package shall not be acceptable. Attached metallic or conductive material shall not be acceptable on the surface of the die if silicon oxide is not visible between at least one metallization strip and the particle. A particle shall be considered attached if it cannot be removed by pushing on it with a pick.

40.6 Bond placement (30X min.) - The base of the wire on the ball bond shall be within the boundaries of the metallization pad and more than one-half of the bond itself shall be on the pad. Bonds shall not extend into an isolation area. The ball bond itself shall not extend into an isolation area by more than 1 mil. Ball bonds shall not overhang the edge of the die nor the peripheral unoxidized silicon. Bonds in the fillet area shall not reduce the major distance between the actual bond area and the edge of the fillet by more than one-half the smallest designed width of the metallization interconnection.

40.7 Scribed die (30X min.) - No die shall be acceptable if silicon oxide is not visible between each pad and the scribed edge of the die.

40.8 Chips (30X min.) - No chip shall be acceptable unless undisturbed oxidized silicon is visible between metallization pad and the edge of the chip. No chip shall be acceptable which appears in the active circuit area or aluminum pads. Reject if ball bond contact area extends over a chip.

40.9 Cracks (80X min.) - Cracks shall not be acceptable which exceed 1.0 mil. in length which point toward an active area, metallization or bonds. Cracks shall not be acceptable which occur in any active area or metallization pad.

40.10 Wedge bonding (30X min.) - Wedge bonds shall be entirely within the confines of the package land flat. Reject if the wedge bond is not at least 1/2 its original size.

40.11 Lead wires (30X min.) - Wire loops displaced greater than three times the diameter of the wire are rejectable. Wires whose tension is so excessive as to cause neckdown greater than 25 per cent of the wire diameter shall be cause for rejection. The completed device shall have no extra leads or lead tail of any length. Leads shall not cross the active portion of the die, nor each other, nor come closer to one another than 2.0 mils at any point.

40.12 Chip bonding (30X min.) - The chip shall be properly oriented in accordance with the applicable assembly drawing and melt shall be visible around at least three sides of the chip. The die shall be attached in an area which is uniform in material and smooth in surface, with no abrupt changes in elevation. The orientation shall be such that no lead wires shall cross, nor any lead wire pass over metallization not electrically common to its pad as a design feature.

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40.13 Package condition (30X min.) - Glass around the header terminals shall be free of foreign material such as gold or conductive materials. General header or case condition shall be clean and free of any material which could possibly become detached during environmental testing. The completed devices shall have no loose particles or other characteristics of poor workmanship.

40.14 Metallization alignment (80X min.) - Metallization alignment shall not be acceptable if 50 per cent or more of the contact window is exposed. Where this tolerance or misalignment is sufficient to allow metallization overlap with, or close proximity to active junction regions and can thus permit channeling or inversion to occur, a reduced misalignment tolerance shall be employed to avoid this condition.

40.15 Exposed junctions (150X min.) - No device shall be acceptable which exhibits any junction area covered only by unithermally oxidized silicon.

40.16 Damaged leads (80X min.) - No device shall be acceptable in which a lead exhibits nicks, cuts, crimps or scoring which cut into or deform the wire by more than 25 per cent of the original diameter.

40.17 Oxide defects - Reject any oxide defect which connects a metal strip with a diffused area not already connected to that strip. Reject any oxide defect which appears to short any two diffused areas. Reject any oxide defect which causes any diffusion area to be discontinuous (except isolation). Reject any oxide defect which exceeds 2 pad areas. Reject any oxide defect whose longest dimension exceeds 1/2 chip width.